region. An insulating film is provided in order to isolate the gate electrode and source electrode (for example, refer to Patent Document 6).

[0012] Also, as another device, the following kind of device is proposed. A vertical power MOSFET includes a) a drain contact provided on one surface of the MOSFET, including a first conductivity type substrate doped to a high level on the drain contact, b) a blocking layer provided on the opposite side of the substrate to the drain contact, including i) a first plural vertical sections, being parallel hexahedrons having six quadrilateral surfaces, that have a horizontal direction thickness shorter than a vertical direction thickness of the blocking layer, wherein ii) P-conductivity type vertical sections and N-conductivity type vertical sections are alternately disposed on the first plural vertical sections, c) a second plural well regions of a second conductivity type opposite to the first conductivity type provided on one surface of the blocking layer on the side opposite to the substrate, d) a first conductivity type third plural source regions doped to a high level, wherein two of the source regions are disposed inside each of the second plural well regions, e) a fourth plural regions of the first conductivity type provided on one surface of the blocking layer on the side opposite to the substrate, wherein each region extends between two well regions of the second plural well regions, and f) a fifth plural gate poly regions, wherein each gate poly region stretches over one source region inside two adjacent well regions and one of the fourth plural regions (for example, refer to Patent Document 7).

[0013] Also, as another device, the following kind of device is proposed. The device includes a first conductivity type first semiconductor layer, a first main electrode electrically connected to the first semiconductor layer, a second conductivity type second semiconductor layer formed inside the first semiconductor layer, disposed cyclically in a lateral direction, wherein the distribution of an amount of impurity in a vertical direction differs from the distribution of an amount of impurity in the vertical direction inside the first semiconductor layer, a second conductivity type third semiconductor layer formed selectively on the surfaces of the first semiconductor layer and second semiconductor layer, a first conductivity type fourth semiconductor layer formed selectively on the surface of the third semiconductor layer, a second main electrode formed so to be joined to the surfaces of the third semiconductor layer and fourth semiconductor layer, and a control electrode formed across a gate insulating film on the surfaces of the first semiconductor layer, third semiconductor layer, and fourth semiconductor layer. The first semiconductor layer has a distribution such that the impurity concentration increases in a vertical direction from the second main electrode toward the first main electrode, while the second semiconductor layer has a distribution such that the impurity concentration is even in a vertical direction from the second main electrode toward the first main electrode (for example, refer to Patent Document 8).

[0014] Also, as another device, the following kind of device is proposed. A semiconductor includes first and second main surfaces, main electrodes provided on each of the first and second main surfaces, a first conductivity type low resistance layer between the first and second main surfaces, and a parallel p-n layer wherein a first conductivity type region and a second conductivity type region are alternately disposed, wherein the impurity concentration in the second conductivity type region on the first main surface side is higher than the impurity concentration in the adjacent first conductivity type region, and the impurity concentration in the second conductivity type region on the second main surface side is lower than the impurity concentration in the adjacent first conductivity type region. The impurity concentration in the second conductivity type region is even in the depth direction, and the impurity concentration in the first conductivity type region on the first main surface side is lower than the impurity concentration in the first conductivity type region on the second main surface side (for example, refer to Patent Document 9).

[0015] Also, as another device, the following kind of device is proposed. The device includes first conductivity type second semiconductor layers and second conductivity type third semiconductor layers alternately disposed on a first conductivity type first semiconductor layer. The device further includes second conductivity type fourth semiconductor layers disposed so as to be in contact with an upper portion of each third semiconductor layer between the second semiconductor layers, and first conductivity type fifth semiconductor layers formed on the surface of each fourth semiconductor layer. The first semiconductor layer is such that a first conductivity type impurity concentration is lower than that of the second semiconductor layers. The third semiconductor layers include a base portion, and portions with a high amount of impurity locally formed in such a way that the amount of impurity in the depth direction is greater than that of the base portion (for example, refer to Patent Document 10).

Related Art Documents

Patent Documents

Patent Document 1: U.S. Patent Document No. 5,216,275

Patent Document 2: U.S. Patent Document No. 5,438,215

Patent Document 3: JP-A-9-266311

Patent Document 4: JP-A-2007-019146

Patent Document 5: JP-A-2006-066421

Patent Document 6: Japanese Patent No. 4,304,433

Patent Document 7: Japanese Patent No. 4,263,787

Patent Document 8: JP-A-2004-119611

Patent Document 9: JP-A-2004-072068

Patent Document 10: JP-A-2006-170598

Outline of the Invention

Problems to be Solved by the Invention

[0016] As a power MOSFET is used as a switching device, there is a demand to, in addition to reducing conduction loss in an on-state, reduce switching loss during switching. The main factors causing an increase in switching loss include, for example, turn-off loss. In order to reduce turn-off loss, it is sufficient to, for example, increase the drain-to-source voltage time change rate (hereafter referred to as turn-off dv/dt) during turn-off. However, increasing the turn-off dv/dt is a cause of noise occurring. Because of this, it is preferable that turn-off dv/dt is low. In this way, there is a trade-off relationship between the turn-off loss and the turn-off dv/dt.